In the Claims

The listing of claims will replace all prior versions, and listing of claims in the application is as follows:

Listing of Claims

1. (currently amended): A method of controlling polysilicon crystallization, comprising the steps of:

forming a heat resist layer on a substrate;

forming a heat sink layer on the heat resist layer ~~a substrate~~, wherein a heat conductive coefficient of the heat sink layer is greater than a heat conductive coefficient of the substrate;

patterning the heat sink layer to form an opening in the heat sink layer, wherein the opening exposes a portion of the ~~substrate~~ heat resist layer;

forming an amorphous silicon layer on the heat sink layer and in the opening ~~substrate~~;

dehydrogenating the amorphous silicon layer; and

laser annealing the amorphous silicon layer to form nucleation sites in the amorphous silicon layer on the heat sink layer, wherein crystallization then grows towards the amorphous silicon layer in the opening to form a polysilicon layer having a grain size of a micrometer with fine grain order.

2. (original): The method of claim 1, wherein the heat sink layer comprises a silicon nitride layer.

3. (original): The method of claim 1, wherein the step of forming the heat sink layer comprises plasma enhanced chemical vapor deposition (PECVD).

4. (original): The method of claim 1, wherein the step of laser annealing comprises using a XeCl excimer laser light source.

5. (original): The method of claim 1, wherein the step of laser annealing comprises laser energy of about 330-450 mJ/cm^2.

6. (currently amended): The method of claim 1, wherein ~~before the step of forming the heat sink layer further comprises forming a heat resist layer, the opening in the heat sink layer exposes a portion of the heat resist layer, and~~ the heat conductive coefficient of the heat resist layer is less than that of the substrate.

7. (original): The method of claim 6, wherein the heat resist layer comprises a silicon oxide layer.

8. (original): The method of claim 6, wherein the step of forming the heat resist layer comprises plasma enhanced chemical vapor deposition (PECVD), physical vapor deposition (PVD), spin coating, or solution-gelation (Sol-Gel).

9. (original): The method of claim 1, wherein between the step of dehydrogenating and the step of laser annealing further comprises forming a heating layer on the amorphous silicon layer, and the heating layer has a semitransparent property for laser light used in the laser annealing.

10. (original): The method of claim 9, wherein the heating layer comprises a silicon oxide layer containing nitrogen and carbon (SiOxNyCz).

11. (original): The method of claim 9, wherein the step of forming the heating layer comprises plasma enhanced chemical vapor deposition (PECVD).

12. (original): The method of claim 1, further comprising the steps of:

forming a gate oxide layer on the polysilicon layer;

forming a gate metal on the opening;

utilizing the gate metal as a mask to implant ions into the polysilicon layer;

forming a dielectric interlayer on the gate metal and the gate oxide layer;

patterning the dielectric interlayer to form contact holes on two sides of the gate metal, wherein the contact holes expose portions of the polysilicon layer;

forming a metal layer on the dielectric interlayer and in the contact holes;

patterning the metal layer to form source/drain metals and a plurality of data lines, wherein the source/drain metals are in the contact holes;

forming a passivation layer on the dielectric interlayer and the source/drain metals;

patterning the passivation layer to form a via hole exposing one of the source/drain metals; and

forming a pixel electrode and a plurality of pixel lines, wherein the pixel electrode is in the via hole to connect the source/drain metals electrically.

13. (original): A method of controlling polysilicon crystallization, comprising the steps of:

forming a heat resist layer on a substrate, wherein a heat conductive coefficient of the heat resist layer is less than a heat conductive coefficient of the substrate;

forming a heat sink layer on the heat resist layer, wherein a heat conductive coefficient of the heat sink layer is greater than the heat conductive coefficient of the substrate;

patterning the heat sink layer to form an opening in the heat sink layer, wherein the opening exposes a portion of the heat resist layer;

forming an amorphous silicon layer on the heat sink layer and in the opening;

dehydrogenating the amorphous silicon layer;

forming a heating layer on the amorphous silicon layer; and

laser annealing the amorphous silicon layer to form nucleation sites in the amorphous silicon layer on the heat sink layer, wherein crystallization grows towards the amorphous silicon layer in the opening to form a polysilicon layer having a grain size of a micrometer with fine grain order.

14. (original): The method of claim 13, wherein the heat resist layer comprises a silicon oxide layer.

15. (original): The method of claim 13, wherein the step of forming the heat resist layer comprises plasma enhanced chemical vapor deposition (PECVD), physical vapor deposition (PVD), spin coating, or solution-gelation (Sol-Gel).

16. (original): The method of claim 13, wherein the step of laser annealing comprises using a XeCl excimer laser light source.

17. (original): The method of claim 13, wherein the step of laser annealing comprises laser energy of about 330-450 mJ/cm^2.

18. (original): The method of claim 13, wherein the heat sink layer comprises a silicon nitride layer.

19. (original): The method of claim 13, wherein the heating layer comprises a silicon oxide layer containing nitrogen and carbon (SiOxNyCz).

20. (original): The method of claim 13, further comprising the steps of:

removing the heating layer;

forming a gate oxide layer on the polysilicon layer;

forming a gate metal on the opening;

utilizing the gate metal as a mask to implant ions into the polysilicon layer;

forming a dielectric interlayer on the gate metal and the gate oxide layer;

patterning the dielectric interlayer to form contact holes on two sides of the gate metal, wherein the contact holes expose portions of the polysilicon layer;

forming a metal layer on the dielectric interlayer and in the contact holes;

patterning the metal layer to form source/drain metals and a plurality of data lines, wherein the source/drain metals are in the contact holes;

forming a passivation layer on the dielectric interlayer and the source/drain metals;

patterning the passivation layer to form a via hole exposing one of the source/drain metals; and

forming a pixel electrode and a plurality of pixel lines, wherein the pixel electrode is in the via hole to connect the source/drain metals electrically.